CLAIMS

What is claimed is:

1. A digital to analog converter comprises:

differential amplifier having a non-inverting input, an inverting input, an non-inverting output, an inverting output, and a gain network coupled to the non-inverting input, the inverting input, the non-inverting output, and the inverting output, wherein the inverting and non-inverting outputs provide an analog output of the digital to analog converter;

plurality of current sources; and

conversion control circuitry operably couples a first set of the plurality of current sources to the inverting input or the non-inverting input of the differential amplifier in accordance with a first set of bits of a digital input and couples, via at least one inversion, a second set of the plurality of current sources to the inverting or the non-inverting input of differential amplifier based on a second set of bits of the digital input.

2. The digital to analog converter of claim 1, wherein the gain network of the differential amplifier further comprises:

a voltage reference source that provides a voltage reference;

a first resistor coupled to the voltage reference source and the inverting input;

a second resistor coupled to the voltage reference source and the non-inverting input, wherein the first and second resistors have substantially similar resistance values;

a third resistor coupled to the non-inverting input and the inverting output; and

a fourth resistor coupled to the inverting input and the non-inverting output, wherein the third and fourth resistors have substantially similar resistance values.

3. The digital to analog converter of claim 1, wherein the plurality of current sources further comprises N number of current sources, wherein each of the N number of current sources provides a same current value, wherein N corresponds to resolution of the analog output.

4. The digital to analog converter of claim 1, wherein the conversion control circuitry further comprises:

a first plurality of switches connected to the plurality of current sources and to the inverting input of the differential amplifier, wherein a number of switches in the first plurality of switches corresponds to resolution of the analog output and wherein a number of current sources in the plurality of current sources corresponds to the resolution of the analog output;

a second plurality of switched connected to the plurality of current sources and to the non-inverting input of the differential amplifier, wherein a number of switches in the second plurality of current sources corresponds to the resolution of the analog output; and

a plurality of cascaded flip-flops interconnected via a plurality of inverters, wherein a number of flip-flops in the plurality of cascaded flip-flops corresponds to the resolution of the analog output, wherein every 2*N flip-flop of the plurality of cascaded flip-flops provides the first set of bits of the digital input, wherein every 2*N - 1 flip-flop of the plurality of cascaded flip-flops provides, via the at least one inversion, the second set of bits of the digital input, wherein N corresponds to the resolution of the analog output.

5. The digital to analog converter of claim 1, wherein the conversion control circuitry further comprises:

a thermometer encoder operably coupled to, in parallel, receive the first and second set of bits of the digital input and to convert the digital input into an encoded digital input;

a plurality of flip-flops each operably coupled to receive a corresponding bit of the encoded digital input, wherein each of the plurality of flip-flops produce an output and an inverted output;

a first plurality of switches, wherein each of the first plurality of switches is operable to connect a corresponding one of the plurality of current sources to the inverting input of the differential amplifier when the output of the corresponding one of the plurality of flip-flops is a logic 1; and

a second plurality of switched, wherein each of the second plurality of switches is operable to connect the corresponding one of the plurality of current sources to the non-inverting input of the differential amplifier when the inverted output of the corresponding one of the plurality of flip-flops is a logic 1.

6. A digital to analog converter comprises:

a plurality of current sources;

differential amplifier module that provides an analog output; and

a plurality of switching modules, wherein each of the plurality of switching modules is operably coupled to a corresponding current source of the plurality of current sources, wherein a first set of the plurality of switching modules couples the corresponding current sources to the differential amplifier module in a first manner based on a digital input value and a second set of the plurality of switching modules couples the corresponding current sources to the differential amplifier module in a second manner based on the digital input value such that, over time, errors introduced by the coupling in the first manner substantially compensate for errors introduced by the coupling in the second manner.

7. The digital to analog converter of claim 6, wherein a switching module of the first set of the plurality of switching modules further comprises:

a flip-flop operably coupled to receive a bit of the digital input value and, when clocked, produce an output corresponding to the bit;

first switch operable to couple the corresponding current source to a first input of the differential amplifier module when the output of the flip-flop is in a first state; and

second switch operable to coupled the corresponding current source to a second input of the differential amplifier module when the output of the flip-flop is in a second state.

8. The digital to analog converter of claim 7, wherein a switching module of the second set of the plurality of switching modules further comprises:

a flip-flop module operably coupled to receive a bit of the digital input value and, when clocked, produce a complimentary output corresponding to the bit;

first switch operable to couple the corresponding current source to the second input of the differential amplifier module when the complimentary output of the flip-flop is in the first state; and

second switch operable to coupled the corresponding current source to the first input of the differential amplifier module when the complimentary output of the flip-flop is in the second state.

9. The digital to analog converter of claim 6 further comprises:

a thermometer encoder operably coupled to receive, in parallel, the digital input value, wherein the thermometer encoder encodes the digital input value into an encoded digital value, wherein the thermometer encoder provides the encoded digital value to the plurality of switches as the digital input value.

10. The digital to analog converter of claim 6, wherein the differential amplifier further comprises:

a non-inverting input, an inverting input, an non-inverting output, an inverting output, and a gain network coupled to the non-inverting input, the inverting input, the non-inverting output, and the inverting output.

11. The digital to analog converter of claim 10, wherein the gain network of the differential amplifier further comprises:

a voltage reference source that provides a voltage reference;

a first resistor coupled to the voltage reference source and the inverting input;

a second resistor coupled to the voltage reference source and the non-inverting input, wherein the first and second resistors have substantially similar resistance values;

a third resistor coupled to the non-inverting input and the inverting output; and

a fourth resistor coupled to the inverting input and the non-inverting output, wherein the third and fourth resistors have substantially similar resistance values.

12. The digital to analog converter of claim 6, wherein the plurality of current sources further comprises N number of current sources, wherein each of the N number of current sources provides a same current value, wherein N corresponds to resolution of the analog output.

13. A method for digital to analog conversion, the method comprises:

receiving a digital signal that includes a plurality of bits;

generating a first signal based on each bit of a first set of the plurality of bits that is in a first state and based on an inversion of each bit of a second set of the plurality of bits that is in the first state;

generating a second signal based on each bit of the first set of the plurality of bits that is in a second state and based on an inversion of each bit of the second set of the plurality bits that is in the second state; and

combining the first and second signals to produce an analog representation of the digital signal.

14. The method of claim 13 further comprises:

generating the first signal as a first current signal;

generating the second signal as a second current signal;

combining the first current signal and the second current signal to produce a current; and

converting the current signal into an analog voltage.

15. The method of claim 13 further comprises:

selecting every 2*N bits of the plurality of bits to comprise the first set of the plurality of bits; and

selecting every 2*N - 1 bits of the plurality of bits to comprise the second set of the plurality of bits.

16. An apparatus for digital to analog conversion, the apparatus comprises:

processing module; and

memory operably coupled to the processing module, wherein the memory further comprises operational instructions that cause the processing module to:

receive a digital signal that includes a plurality of bits;

generate a first signal based on each bit of a first set of the plurality of bits that is in a first state and based on an inversion of each bit of a second set of the plurality of bits that is in the first state;

generate a second signal based on each bit of the first set of the plurality of bits that is in a second state and based on an inversion of each bit of the second set of the plurality bits that is in the second state; and

combine the first signal and the second signal to produce an analog representation of the digital signal.

17. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to:

generate the first signal as a first current signal;

generate the second signal as a second current signal;

combine the first current signal and the second current signal to produce a current; and

convert the current signal into an analog voltage.

18. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to:

select every 2*N bits of the plurality of bits to comprise the first set of the plurality of bits; and

select every 2*N - 1 bits of the plurality of bits to comprise the second set of the plurality of bits.